

CSP Assembly Reliability

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California
818-354-2059
Reza.Ghaffarian@JPL.NASA.Gov

INTRODUCTION

This section reviews the many factors that affect interconnect reliability of emerging chip scale package (CSP) assemblies. These include: package type, package build, board design, and assembly variables. Methods of accelerated environmental testing were discussed and reasons for unrealistic life projections for CSP assembly reliability by numerous modelers are also examined. It also presents our experience in the areas of technology implementation challenges, including design and building both standard and microvia boards, and assembly of two types of test vehicles. We also discuss package isothermal aging test results performed at 100°C and 125°C to 2,000 hours. Preliminary thermal cycling test results in the range of -30°C to 100°C for trial test vehicles and full production, especially comparison of single sided assemblies to double sided assemblies were also presented.

INDUSTRY AND “EXPERT” DEFINITION OF CSP

Although the expression “CSP” is widely used by industry both suppliers and users, its definition had evolved as the technology has matured. At the start of the package’s introduction into the market, a very precise definition was adopted by a group of industry experts. CSP was defined as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Soon, it became apparent that suppliers were using the term CSP to promote a miniature version of a previous package.

A rapid transition to a much lower size was difficult both for package suppliers and end users. Suppliers had difficulty in building such packages whereas the users had difficulties in accommodating the need for the new microvia printed circuit board (PWB), chiefly, because of routing requirements and its increased cost. Other issues for accepting the “interim definition” by industry included needed maturity in assembly and infrastructure. For example, the use of pitches other than 0.5 mm, including 0.75 and 0.65, was aimed at using a standard PWB design rather than a microvia build to avoid the elevated cost of the latter.

The “expert definition” undermines one of the key purpose of the packages allowing for die shrinkage. If die shrinkage is acceptable for the package to retain the footprint, then a decrease in die size for the same CSP will change the term CSP for that package.

Therefore, in reality, CSPs are miniature new packages that industry is starting to implement, and there are many unresolved technical issues associated with their implementation. Technical issues themselves also change as packages mature. For example, in early 1997, packages with 1 mm pitch and lower were the dominant CSPs, whereas in early 1998 packages with 0.8 mm and lower became the norm for CSPs. New issues included the use of flip chip die rather than wire bond die in the CSP. Flip chip failure within the package is a potential new failure mechanism that needs to be considered.

CSP RELIABILITY CHALLENGES

Emerging grid Chip Scale Packages (CSPs), miniature version of ball grid arrays (BGAs), are competing with bare die flip chip assemblies. CSP is an important miniature electronic package technology for utilizing especially low pin counts, without the attendant handling and processing problems of low peripheral leaded packages such as thin small outline packages (TSOPs) and high I/O (input/output) quad flat packages (QFPs). Advantages include self alignment characterization during assembly reflow process and better lead (ball) rigidity. Reliability data and inspection techniques are needed for its acceptance especially for high reliability applications.

Reliability, irrespective of its definition, is no longer an “after-the-fact” concept; rather, it must be an integral part of development and implementation. This is specifically true for microelectronics with demands for miniaturization and system integration in a faster, better, and cheaper environment. CSPs rapid development and introduction into the market is a good example of this trend.

The use of new materials, processes, and new applications obscure the traditional definition of quality and reliability assurance. New systems approaches are needed to assure quality and reliability as well as to manage risks. Quality should be assured by design for reliability, controls for processes, tailored testing methods for qualification, and use of unique accelerated environmental testing along with credible analytical prediction. In other words, an efficient concurrent engineering system approach must be implemented.

Environmental Testing

Among the many environmental accelerated testing methodologies for assessing reliability of electronic systems, thermal cycling is the most commonly used for characterization of devices as well as interconnections. Among the many predefined thermal cycling profiles, the military and commercial aspects represent the two extremes. Previously, NASA also had a preset specific thermal cycling requirement. The Military Standard 883 (Mil-STD-883) defines different accelerated thermal cycling which are generally used as benchmark testing. Within Mil-STD-883, there are three levels of cycling temperatures:

- Condition A, -55°/85°C
- Condition B, -55°/125°C
- Condition C, -65°/150°C

For benchmark conditions, devices are generally subjected to condition C and assemblies most often to condition B. The assemblies were traditionally considered qualified when they last 1,000 cycles. A commercial cycling profile, the J-12 IPC specification, recommends a thermal cycle in the range of 0°C to 100°C. Within a temperature range, the dwell, heat and cool down rates are critical parameters and also affect cycles to failure.

The NASA thermal cycling requirements are stringent and are specified in various revisions of NASA Handbooks. For example, in a previous revision, NHB 5300.4 (3A-1), there was a well defined requirement for number of cycles and solder condition after exposure. No cracking of any solder joint was allowed after 200 NASA cycles (-55°C to 100°C with 245 minutes duration).

Performance-Based Assurance Requirement

In a subsequent NHB revision, the requirements were based on meeting the specific mission condition. The build and test methodology is expected to yield confidence in reliability to satisfy the mission conditions. Mission requirements are emphasized rather than a universal cycle and a value for all missions.

Test to “establish the confidence in reliability” adopted by NASA a long-time ago is now “the reliability theme” for the commercial sector. Discussions on “Breaking Traditional Paradigms” and “Rethinking of Environmental Reliability Testing” by authors from the commercial sector are becoming hot topics with the introduction of new miniaturized CSPs. CSPs have their own unique form factor not seen in SMT. Unable to meet the stringent requirements established by the previous military standards, a new “paradigm shift” is considered to be the solution. The “shift” is further motivated by several factors including the following:

- Reduction in life expectancy for consumer electronics
- Rapid changes in electronic technology
- Obsolescence of many military specifications

Additional unique tests are now adopted to meet the specific consumer electronic products. For portable electronics, bend test, drop test, and possible “washing machine test” are suggested. The IPC 9701 specification, Qualification and Performance Test Methods for Surface Mount Solder Attachments, is aimed to include some of these requirements. It must be recognized that no accelerated tests can be truly universal. Field reliability is the ultimate test, and either substantiates or invalidates the experimental tests.

For space missions, gathering information on the root cause field failure is almost impossible. For commercial applications, rapid changes in technology render field information almost useless for new product development. The only solution is to understand key reliability parameters and to design for reliability. Subsequent process controls, as well as efficient qualification and inspection, also help assure sufficient field reliability. In other words, risk control and risk management must be practiced.

Microelectronics Assembly Reliability

For surface mount, solder has both electrical and mechanical functions. Thus for SMT, damage to solder could readily affect functional integrity of the system. Therefore, defects that cause changes either in mechanical or electrical system characteristics and their reasons for failure are critical. The most common damage to solder joints are those induced by thermal cycling. The main cause of such damage is considered to be differences in thermal expansion of package and PWB materials. This is especially true for eutectic solder (63Sn/37Pb) which creeps at room temperature.

Creep for materials generally occurs at temperatures above half of the absolute melting temperature ($T/T_m > 0.5$). This value is 0.65 at room temperature for eutectic solder. Creep and stress relaxation are main causes of cycling damage.

Thermal cycling induced damages are expected to increase even more with the trend toward energy conservation. Powering down whenever the system is not actively used results in more cycles. Previously, electronic hardware was generally left on for long periods of time which resulted in relatively few thermal cycles. The on-off demand raises more concerns regarding solder joints which are affected by thermal cycling. Thermal damage to solder joints are most often caused by the followings:

- Global CTE (Coefficient of Thermal Expansion) mismatch between the package and board induces stresses. The package and board can also have temperature gradients through the thickness and at surface areas
- Local CTE mismatch between solder attached to the component and the PWB

Reducing the CTE mismatch of component and PWB reduces cycling damages, but the ideal condition depends on thermal conditions of the component, PWB, and solder. An ideally CTE matched condition could be a tailored PWB material with a slightly higher CTE value than the component. This is based on the assumption that the global CTE mismatch is dominant, and the component with the heat generating die is hotter than the PWB.

There are other approaches to reducing damage to solder joints. Underfill application is a common technique which has been widely used for direct attachment of chip on board or when package leads are not robust. Other less conventional approaches are aimed at absorbing CTE mismatch between the die and board within the package or externally through strain absorbing mechanisms, and therefore reducing stresses on the solder interconnects. These approaches could introduce their own unique damage since the weakest link now is transferred from solder to other areas of the attachment system.

Tests Methods for Reliability Evaluation

Thermal cycling and a series of other environmental tests have been commonly used to gain confidence in reliability of SM packages and assemblies. There are also additional tailored tests for specific applications. For space applications, vibration and shock representation of launch is an example of a tailored experiment. For portable products, new tests are being carried out. Bend, drop, and perhaps “washing machine” tests are especially important. It is interesting to note that these tests are devised to meet the harsh environment generated by human mishandling. Even though, some of these tests might not have any scientific basis, but it meets customer perception of quality and reliability of products and might become a reality.

Literature Data on CSP Assembly Thermal Cycling

Tables 1-3 show thermal cycles to failure under different conditions for various CSP assemblies with low to high I/Os. Except for μ BGA™, most other test results are from package manufacturers. Although manufacturer data on assembly are valuable, they are probably have been generated for chosen packages under extreme materials and process controls and they might not represent a user application requirements.

Note from the Table 1 that for μ BGA™, two users showed 1,000 and 500 failure cycles in the range of -55°C to 125°C. The higher value possibly were from a more controlled environment whereas the lower value represented a mix of different supplier licensees for this package. Recent assembly test data by manufacturer (private communication, July '99) indicate that the assemblies survived 1,000 and 600 thermal cycles in the range of -40°C/125°C and -65°C/150°C, respectively. Among the grid array packages, the JACS-Pak™ is the only package which shows higher than 1,000

cycles to failure in the range same temperature range (-55°C/125°C). Ceramic CSP (CCSP) data generated by manufacturer showed closer reliability to plastic CSP than their SM versions. Reasons for CCSP assembly reliability improvements may include reduction in package size and thickness. Strain induced on the ceramic joint directly relates to size or Distance to Neutral Point (DNP). Note again that these data were generated by suppliers and there are no independent validation tests by others as yet.

Wafer level assemblies have often showed very low cycles to failure and most required underfilling to have comparable reliability to conventional SM packages. Leaded CSPs, with low I/O generally have comparable reliability to their SM counterparts as shown in Table 3. There is a large difference between the two independent sets of data for TSOP (Thin Small Outline Package). The two extremes are 200 and 2,200 failure cycles in the range of -55°C to 125°C.

A recent assembly characterization by a user revealed much valuable information (K. Newman, Chip Scale International '98). Most packages failed early and did not meet the user requirement for cycles to failure. Only two out of eight packages, from six manufacturers, passed the user failure free cycles requirement. Acceptable failure-free cycles was 3,500 cycles for thermal cycling in the range of 0°C to 100°C. The results were at least an order of magnitude lower than those for Plastic BGAs (PBGAs). Failures lower than 1,000 cycles, even in the range of 0°C to 100°C, is a good indication of package immaturity at the time of evaluation (late 1997).

It is difficult to determine if use of underfill might have relieved these early failures since no information by package manufacturers was given. Detailed failure mechanism analyses might have revealed that use of underfill would have reduced the number of failures. Underfilling was considered to be unacceptable because adding additional assembly steps.

Dynamic behavior of CSPs are critical especially for portable products where there are potential of human mishandling such as accidental drop. Favorable Test results are given for a few packages reported in literature. For example, the UltraCSP™ (P. Elenius, Pan Pacific, '99) was dropped from the height of 1600 mm, achieving a mechanical shock of 8200 G over period of 0.12 msec with no failure during mechanical shock. No failure was also observed when the drop height increased to 2000 mm with a mechanical shock of 12,500 G over a period of 0.11 msec. Intel reported mechanical shock test results for µBGA™ (R. Bauer, J. Mlatasta, SMI '98) using Mil Std 883. Fifteen samples were subjected to 1500 g with 0.5msec duration in the X, Y, and Z. No failure was observed after five shock pulses. It also showed no failure due to four cycles of vibration in 20-2000 HZ with a 20 g maximum load.

Literature Survey on Variables Affecting CSP Reliability

There are many factors that affect CSP reliability. These include design, package build, solder paste, assembly, underfill, and type of test for reliability evaluation. In the following a few of these variables are discussed.

Design

- PWB pad design; NSMD (non-solder mask) is now commonly recommended. For BGAs, discussions on use of solder mask defined vs. non-solder mask (SMD vs. NSMD) were hot subjects for a short period. There were two camps, one showing the improvement due to use of SMD— reasoning that masks over copper are needed for improved adhesion as well as the potential benefit of cycles to failure increased due to increase solder joint height. The other camp showed that crack initiation in solder, due to overlaying of the mask, could reduce the number of cycles to failure.

The pad size design relative to package has its own supporters. As a rule of thumb, the board pad size should be the same as the package. A slight unbalance in this relationship could result in failure at the board or package. Optimized conditions might differ for different packages depending on the ball attachment configuration.

Package Variables

- Die bond on interposer; There are various techniques for transferring the die I/O to the interposer within the package. Each element of the package internal form has its own effect. For the TAB CSP (Tape Automated Bonding), the TAB might be the weakest link. Generally, CSPs and BGAs with flip chip dies are more susceptible to internal package failure than their wire bond versions. For the flip chip die in JACS-Pak, the failure was observed on the C5 (board level) solder joint interconnection, when subjected to thermal cycling.

- Interposer thickness; When the interposer was increased from 0.4 mm thickness to 0.6 mm, cycles to failure increased from 400 to about 800 cycles (-25/125°C). Data for JACS-Pak™, indicates that semi-rigid interposer would have 1.88 times the number of thermal cycles. Is the rigidity equivalent to thickness change or possibly because of materials change? The answer is not known. Interposer CTE also has significant affect on the board reliability.
- Interposer materials- CSPs with different interposer materials showed significantly different cycles to failure— about a three times increase (Sony, IMAPS '97). In an experiment, it was found that a factor of about three times will be achieved when a low CTE interposer was used (1200 vs. 400 cycles, -25/125°C).
- Die size; In one study it was shown (Amkor, ECTC 98) that when die size increased from 6.4 mm to 9.5 mm, the first cycles to failure decreased from 1500 to 900 cycles in the range of -40°C to 125°C.

Solder Ball

- Solder composition; Eutectic solder (63/37) is the most commonly used solder due to it having many desirable attributes, including low temperature melting. To improve fatigue characteristics, small amounts of silver (2%) have been added to this composition. Additive materials have the potential of formation of brittle intermetallic phases as well as softening by precipitation formation. These metallurgical transitions are further accelerated by increases in temperature. Effect of five element alloy was shown to improve thermal cycling reliability by 1.2 to 1.5 times (TI, SMI '97).
- Ball shape attachment; For BGAs, it has been demonstrated that the DBGAs (Dimple BGA) improve reliability. This might be the case for CSPs too, but its significance is yet to be demonstrated.

Assembly Variables of Reliability

- Solder joint height; The effect of solder joint height on reliability has been widely discussed for BGAs. One reason for the use of an SMD pad for PBGAs, with collapsible solder, was to increase solder ball height and hence increase reliability. Height was also increased by use of columns in the ceramic column grid arrays to achieve significant reliability improvements compared to the ball grid array version. Improvement was shown for CSPs when ball heights are increased (Sony, IMAPS 97).
- Underfill; One key advantage of CSPs over flip chips is that ideally there is no requirement for CSPs to be underfilled. The assemblers for consumer products prefer packages with no underfill one process step is eliminated and reworkability is permitted. However, for high reliability applications where vibration and shock are key in ruggedness, use of underfill might be the only solution now known to meet the harsh requirements.
- For flip chips with very short cycles to failure, it has been shown that underfill will improve cycles to failure reliability an order of magnitude (5-10 at least). This is very similar to the results shown in Table 2 for the wafer level miniBGA packages with and without underfill.
- Double Reflow; There are many concerns when double sided boards are assembled. Reliability reduction is one. For heavy BGAs, one concern was potential part fall from the assembled side during the second reflow. Similar concerns might be true for CSPs with the small solder volume; not enough tension force to hold even the small size of CSPs. In addition, it has been shown that for two sided packages, reliability of board assembly was half of the single sided (Sony, IMAPS '97). Recently, similar test results were presented for another CSP package (Sharp, ECTC '98). Double sided assemblies with packages on directly opposite sides of the board showed lower cycles to failure. This was improved with partial relative package offsets on the two sides.

Failure Mechanisms and CSP Reliability

Solder joint interconnects were considered to be the main cause of assembly failure. Failure at the board level could also be caused by the internal failure of the package. For example, package internal TAB lead failures at heels were reported for the CTE absorbed CSP—a fatigue failure shift from the solder joint to the internal package (see Table 1). This new type of failure is in contrast to the traditional theoretical wisdom where the solder joint failure is generally considered to be the weak link in solder joint assemblies. This and other failure mechanisms, which are being established for CSPs, must be understood by a modeler before he/she is to predict a meaningful reliability projection.

Table 4 includes four projections from different modelers and experiment test results. It is interesting to compare the theoretical values with those experiment test results for numerous CSPs. It becomes obvious that these calculations are at least 5 to 20 times higher than the test results. As noted earlier, the highest value test results are in the range of 1,000 to 1,500 cycles. Projections of more than 20,000 cycles to failure in the range of -55°C to 125°C are highly unrealistic values.

Unrealistic modeling results could also occur when DNP is used as indicator for cycles to failure. In the IPC report J-STD-012 (Joint Industry Standard Implementation of Flip Chip and Chip Scale Technology), assembly reliability projections were based on flip chip die being attached to the board. DNPs were suggested to be used for calculation of the first failure and projection of failure with size of package. This is not valid for most CSPs, except possibly for a few wafer level CSPs without underfill. Although there is a relationship between an increase in die size and reliability, the relationship is not linear and depends on many parameters. For example, fan-out packages with small die will not follow the DNP indications.

Table 4 Misleading CSP Cycles to Failure Projections by Modeling

Package Type	I/O	Cycle Profile	Cycles to Failure Projection	Test Results
TAB CSP	46	-55/125°C	7,000	500-1,000
WAFER CSP	96	-40/125°C	3,200	200-500 8 failures
FLIP CHIP CSP	N/A	-55/125°C	20,000	N/A
LOW COST CSP	N/A	-40/125°C	21,000	N/A

CSP IMPLEMENTATION CHALLENGES

The JPL-led CSP consortia of enterprises representing government agencies and private companies have jointed together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. In the process of building the JPL-led consortia test vehicles [1], numerous challenges were identified. The thought processes for the first test vehicle started in late 1996, when very few packages were available for evaluation. The design for the second test vehicle initiated in mid 1998, when a much larger number of CSPs were available, estimated to be nearly fifty types. Although CSPs' rapid growth has eased package availability, its implementation, especially for high reliability applications, requires establishment of many technical issues including assurance for quality and confidence in reliability, as well as development of the necessary infrastructure.

In the following, key challenges for package and PWB design, and assembly of test vehicles will be presented. Also, the most update environmental test results for CSPs and their assemblies will be given.

Package Availability in Early 1997

CSP availability in daisy chain for the attachment reliability characterization was one of the challenging issues at the start of the program in early 1997. There were numerous publications on a wide range of CSPs, but most packages were in an early development stage and lacked package reliability information. Assembly reliability data were even rarer. Most packages were only available in prototype form, and this, of course, did not guarantee any similarity to the production version, or even the future availability of the package.

More than a six month delay in package delivery date was the norm. Four packages were not delivered at all, and one was delayed almost a year with a last moment modification by the supplier. Although many suppliers promoted their packages and package reliability, they were not willing to submit their packages for an independent evaluation, possibly because of lack of confidence.

At the start of the program, I/Os ranged from 12 to 540 to meet the short and longer term applications. The 540 I/O/ 0.5 mm package was dropped by the manufacturer prior to the trial test vehicle assembly. Three other higher I/O with 0.5 mm pitch were not delivered. For example, a hard metric, 0.5 mm CSP package with 188 I/Os having reliability data given by the supplier for its English pitch version was among these three packages. The supplier was unable to meet our last build scheduled in late 1998.

Lack of delivery clearly indicate that the package suppliers were struggling to build CSPs with 0.5 mm pitch, especially with high I/O counts. Therefore, by default, the maximum I/O package became a CSP with 275 I/Os.

The majority of the CSPs of the next phase of the CSP program have pitches of 0.8 mm. In this phase, there are a few high I/O CSPs with 0.5 mm pitch. This indicates that industry is starting to be more comfortable with moving towards a tighter pitch at higher I/O.

Lack of Design Guidelines

Guidelines and standards on various elements of CSPs were not available. For example, there was missing package daisy chain information, and insufficient mechanical drawing data to begin with. The majority of packages were hard metric, however, a few with the inch pitches caused dimensional errors when converted from inch to metric. Furthermore, ball and pad information needed for board design was missing and it was time consuming to gather information from suppliers since most needed to be generated by technical personnel. There was no information on pad design relative to package pad for achieving optimum reliability. Pads for PWBs could be assumed to be the same as package, as a rule of thumb. For our design, guidelines developed by the package suppliers were used when available. Otherwise, available knowledge and engineering judgment were utilized.

Need for Microvia PWB

The standard PWB design could be used for low I/O CSPs. Build up (microvia) board technology is required for higher I/O CSPs in product with active die. For daisy chain packages, it is possible to design high I/O on a standard board. Board design guidelines are needed, especially for the build up (microvia) configuration.

I/O Limitation

There were a number of packages from low I/O (<50) to higher I/Os (about 500) for characterization. It became apparent that for the near future, 1-3 years, the dominant packages would be those with less than 50 I/Os. Specific application requirements could utilize packages with much higher I/Os. Mixture of conventional SM (surface mount) packages including, TSOP, flip chip die, BGAs, fine pitch BGAs, and CSPs on one board is another expected design and assembly challenge. This mixed technology is being considered for the next test vehicle under the second JPL-led CSP Consortium.

CSP Test Vehicle Design

The Consortium agreed to concentrate on the following aspects of CSP technology after numerous workshops, meetings, and weekly teleconferences.

Package — Ten packages from 28 to 275 as listed in Table 5. The TSOP was used as control.

Printed Wiring Board (PWB) Materials and Build — Both FR-4 and BT (Bismaleimide Triazine) materials were available in the resin copper coated form for evaluation. High temperature FR-4 and Thermount® were also included. The boards were double sided, standard and microvia. With our test matrix design, direct reliability comparison between the two board technologies as well as double side processing is possible. In designing daisy chains, it became apparent that the standard PWB technology could not be used for routing the majority of packages.

Table 5 CSP Package Configurations Matrix

Package ID	Package Type	Package Size (mm)	Pad Size (mm)	Pitch (mm)	I/O Count	Package Thickness (mm)	Ball Dia (mm)
A	Low I/O Wafer	1.6 x 3.2	0.25 x 0.15	0.5	12	0.5	0.075
B	Leadless-1	7 x 13.6	0.35 x 0.7	0.8	28	0.8	-
C	TAB CSP-2	7.43 x 5.80	0.4	0.75	40	0.885	0.3
D	TSOP44	18.61 x 10.36	0.27 x 0.5	0.8	44	1.13	n/a
E	Leadless-2	7 x 12.3	0.30 x 0.75	0.5	46	0.8	n/a
F	TAB CSP-1	7.87 x 5.76	0.4	0.75	46	0.91	0.3
G	Chip on Flex-1 (COF-1)	0.3" x 0.3"	.010 in.	.020 in.	96	1.75	0.3
H	CSP-Redistribution-1	10.025 x 8.995	0.254	0.5	96	-	0.3
I	CSP-Redistribution-2	6.22 x 5.46	0.254	0.5	99	-	0.3
J	Wire Bond on Flex-1	12.1 x 12.1	0.375	0.8	144	1.4	0.5
K	Wire Bond on Flex-2	12 x 12	0.25	0.5	176	0.5	0.3
L	TAB CSP-3	13.1 x 13.1	0.3	0.5	188	0.5	0.3
M	Chip on Flex-2 (COF-2)	0.5 x 0.5	.010 in.	.020 in.	206	1.75	0.3
N	Ceramic CSP	15 x 15	0.4	0.8	265	0.8	0.5
O	Wafer Level	0.413 x 0.413	.010 in.	.020 in.	275	-	0.3

* All measurements are in mm unless otherwise specified

Daisy Chain — Packages had different pitches, solder ball volumes and compositions, and daisy chain patterns. In most cases, these patterns were irregular and much time and effort was required for design. This was especially cumbersome for packages with higher I/Os and many daisy chain mazes were developed.

Surface finish — At least four types of surface finishes were considered. Organic solder preservative (OSP), hot air solder leveling (HASL), Au/Ni (two thicknesses), and immersion silver; the majority were OSP finish. Three types of solder pastes were included: no-clean, water soluble (WS), and rosin mildly activated (RMA).

Underfill — Packages with underfill requirements were included both with and without underfill to better understand the reliability consequence of not using underfill.

Double Sided Assembly — PWBs were double sided and several boards with double sided packages were assembled to investigate the reliability of single sided versus double sided test vehicles, as well as standard versus microvia technology.

Solder Volume — Three stencil thicknesses were included: high, standard, and low. The two extreme thicknesses were 4 and 7 mils with different stencil aperture design depending on the pad size. The standard which was used for the majority of test vehicles was 6 mil thickness.

Test Vehicle Feature — The test vehicle was 4.5 by 4.5 inches and divided into four independent regions. For single side assembly, most packages can be cut for failure analysis without affecting the daisy chains of other packages. All packages were daisy chained and they had up to two internal chain patterns.

Environmental testing — To link the data to those generated for the Ball Grid Array Consortium test, two conditions of –30° to 100°C (cycle A) and –55° to 125°C (Cycle B) were included. Two additional cycles were also investigated. Thermal cycling in the range of 0° to 100°C was performed to meet the needs of the commercial team members.

Hence, four different thermal cycle profiles were used. These were:

- Cycle A: The cycle A condition ranged from –30° to 100°C and had an increase/decrease heating rate of 2° to 5°C/min and dwell of about 20 minutes at the high temperature to assure near complete creep of the solder. The duration of each cycle was 82 minutes.

- Cycle B: The cycle B condition ranged from -55° to 125°C , with a very high heating/cooling rate. This cycle represent near thermal shock since it utilized a three region chamber: hot, ambient, and cold. Heating and cooling rates were nonlinear with dwells at the extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.
- Cycle C: The cycle C condition ranged from -55° to 100°C with a short time duration at low temperature. The heating and cooling rates were 2° to 5°C/min with a dwell at maximum temperature of more than 10 minutes.. The duration of each cycle was 90 minutes.

Cycle D: The cycle D condition ranged from 0° to 100°C with a $2\text{-}5^{\circ}\text{C/min}$ heating/cooling rate. The Dwell at the extreme temperatures was at least 10 minutes, the cycle duration was 73 minutes.

Monitoring — The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC-SM-785, Sect. 6.0, were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, there were many additional interruptions within 10% of the cycle life.

ISOTHERMAL AGING CSP/BGA PACKAGES

This investigation included isothermal aging of BGA as well as grid CSP packages to determine degradation of ball/package with temperature and time as well thermal cycling. Other objectives were to determine if there were differences in package/ball interface integrity for different package before and after isothermal exposure and if this correlated with cycles to failure test results. The isothermal temperatures were the maximum thermal cycling temperatures.

BGA Assembly Failure From Ball/Package

For BGA, assembly joint failures either between ball and package or ball and PWB (solder joint) were observed after thermal cycling. For grid CSPs, the interface between package and solder balls is also a potential failure site.

For BGAs, cycles to failure and failure mechanisms under different environments were investigated under another program [2]. Figure 1, adapted from Reference 2, shows cumulative failure percentages versus increasing cycles for several plastic BGA assemblies. Wider distribution for two peripheral BGA packages can be seen in this figure.

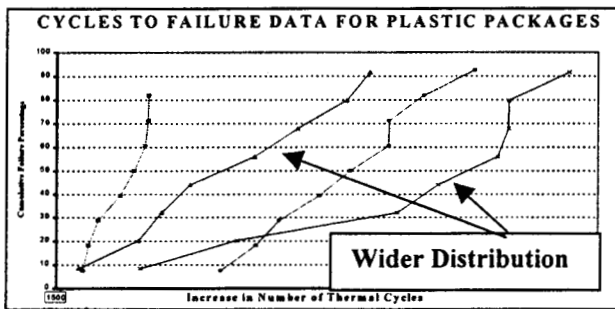


Figure 1 Wide Distribution for Two BGA Package Types

The exact causes of wider distributions are yet to be identified. Possible causes include: PWB materials (FR-4, polyimide), solder volume, and ball/package metallurgy/integrity. Package/ball integrity plays a role since failure analyses of cycled BGA assemblies indicated that failures occurred either at package or board interfaces. In addition, up to a 50% reduction in strength was found when another type of BGA build was subjected to isothermal aging for 1,000 hours at 125°C . It is not known if this large reduction was an exception because of build configuration or if it would be true for other widely used BGA configurations.

Test Procedures

Both plastic and ceramic BGAs, with their thermal cycling behavior already characterized, were subjected to shear testing before and after isothermal aging exposure. The grid CSPs were from the Table 1 list.

Both BGA and CSP packages were subjected to visual inspection and scanning electron microscopy (SEM) to characterize their joint quality, solder ball metallurgy, and elemental compositions. In addition, several assemblies from a grid CSP were subjected to pull tests before thermal cycling and after at 1,500 cycles (-30 to 100°C).

Ball Shear Prior to Isothermal Aging

Figure 2 shows as-received cumulative percentage versus shear forces for various BGAs and grid CSPs. The median ranking ($i-0.3/n+0.4$) was used to calculate cumulative percentages. The fifty percentile shear forces as well as their respective shear stresses are shown in Table 6.

Shear forces ranged from 170 to about 400 grams for CSPs and from about 1,000 to 1,500 grams for plastic and ceramic BGAs. Shear force depends on many variables including the pad size, metallurgy, and configuration attachment as well as chemistry of solder. Shear behavior become critical for application under mechanical conditions.

Shear stresses were calculated based on the sheared surface areas and had a much narrower range for both CSPs and BGAs. They ranged from 3.8 to 5.7 kgrm/mm² except for a grid CSP with value of 7.6 kgrm/mm². This might be due to solder metallurgy as well as ductile failure during shear testing.

It is interesting to note the significant difference in shear forces for different packages. Distributions for the same packages from different suppliers were only slightly different. The CSP-2 with non clearance mask had a tighter force distribution.

Table 6 Shear force and stress for various CSPs

Package Type	I/O	Shear Diameter (mm)	Shear Force (grm) at 50%	Shear Stress (kgrm/mm ²)
TABCSP-1	46	0.320	376	4.7
TABCSP-2	40	0.30	397	5.7
Wafer CSP	275	0.250	185	3.8
Grid CSP	176	0.170	172	7.6
PBGA	256	0.60	1088	3.8
PBGA	313	0.575	1100	4.2
PBGA (OMPAC)	352	0.60	1159	4.1
SBGA	352	0.555	1128	4.7
SBGA	560	0.540	1020	4.5
CBGA	361	0.645	1530	4.7

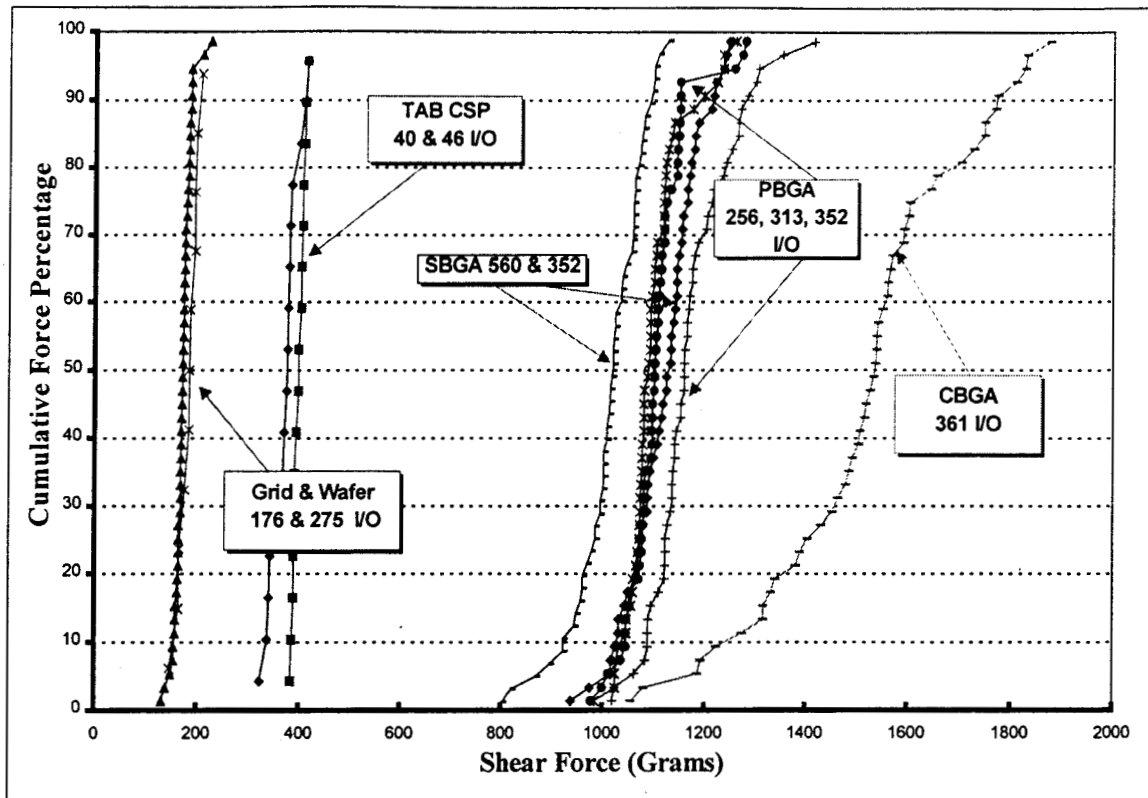


Figure 2 Ball/Package Shear Force Distribution for Various CSPs

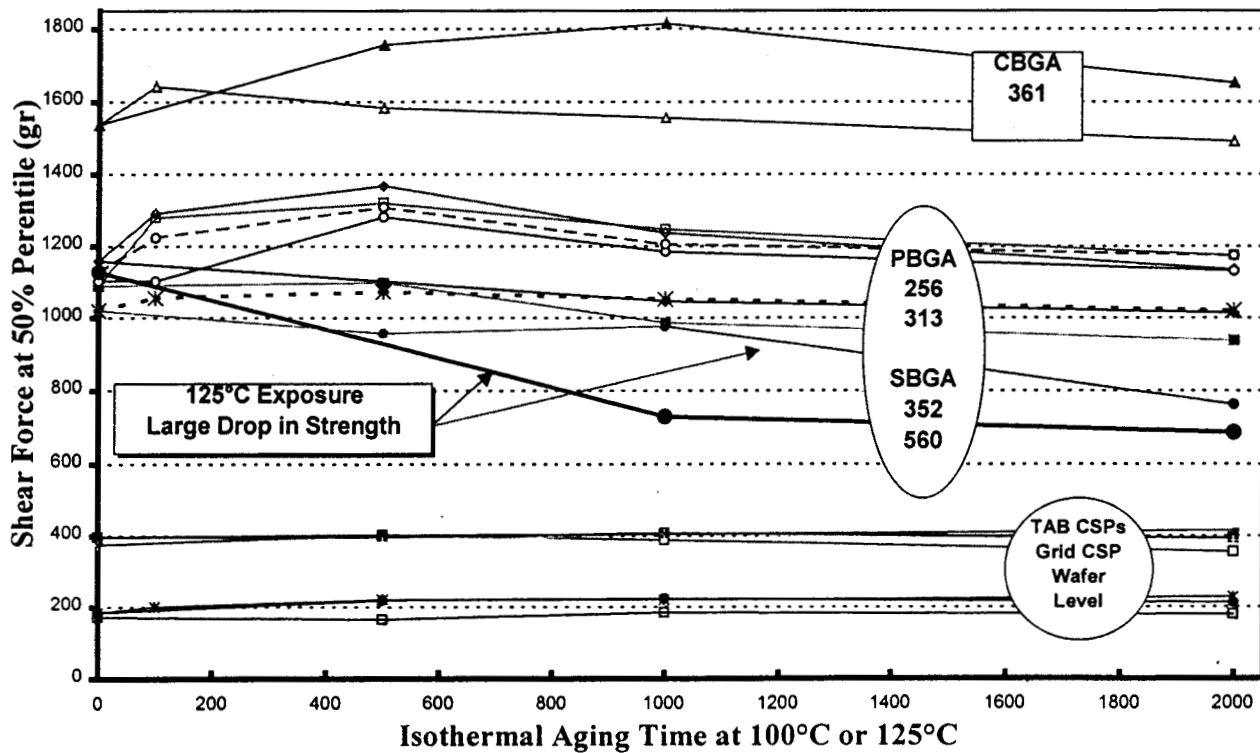
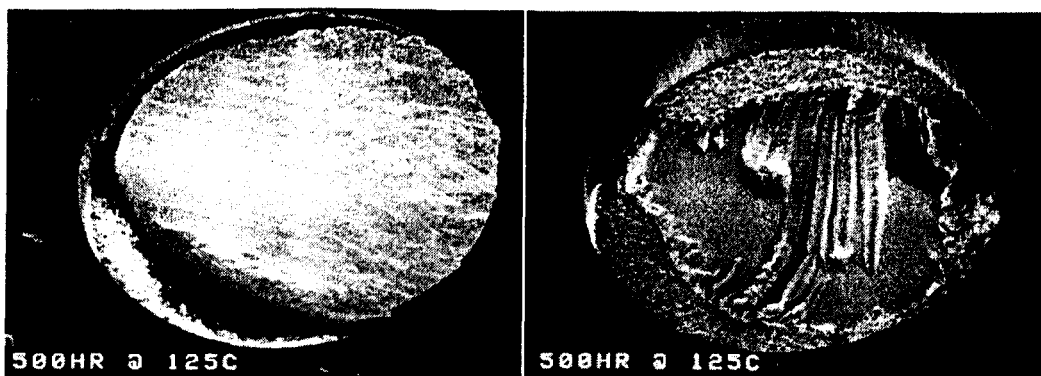
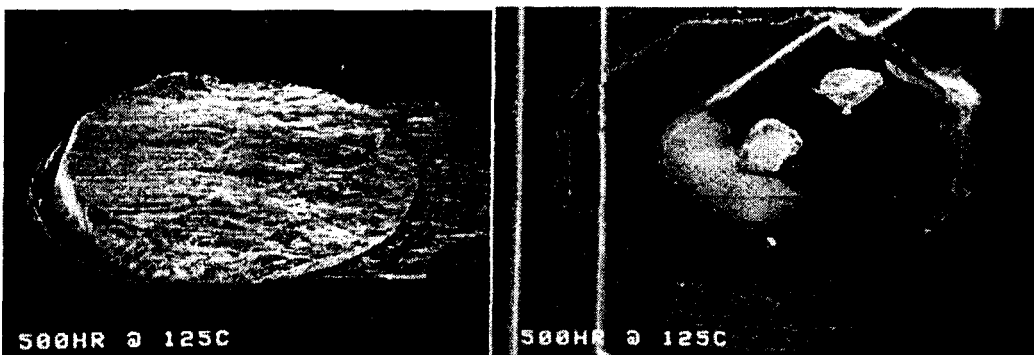


Figure 3 Ball/Package Shear Forces (N50%) vs. Time for Isothermal Aging at 100 and 125 °C for a Number of CSP and BGA Packages



(a) SEM Photomicrographs of Failure Surface after 500 hr at 125 °C and Shear Test for TABCSP-1



(b) SEM Photos Failure Surface after 500 hr at 125 °C and Shear Test for TABCSP-2 (left) and Wafer level

Figure 4 SEM Photos of Failure Surface after Isothermal Aging Various CSPs

Isothermal Aging

Figure 3 shows the 50% shear force values (N50%) for both BGA and CSP packages tested at 100 and 125°C to 2,000 hours. There are three distinct regions: CSPs, PBGAs, and CBGAs. In general, irrespective of package types, shear forces increased with aging initially and dropped slightly at higher aging times.

Shear data without the record of failure mechanism might be of no value. For example, the wafer level package showed improvement after exposure. The most probable cause of improvement after exposure at 100°C is microstructural changes which could have reduced the processing residual stresses. However, improvement after exposure at 125°C, at least for one case, is meaningless, since improvement was due to a failure mode change— from ball/package interface failure to tearing after exposure because of significant package build up degradation (see Figure 4).

The two SBGA packages showed a different trend. Shear forces decreased with increasing aging times and about 40% dropped after 1,000 hours. Note that the SBGAs were from an early production version [2]. Assemblies for both BGAs had wide distribution. The widest distribution was for PBGA 256 having the same trend as other BGAs.

TRIAL TEST VEHICLE ASSEMBLY RELIABILITY

The Consortium assembled thirty #1 test vehicles (TV) and seven trial #2 test vehicles and nearly 200 #2 full production. Grid CSPs are known to be robust in manufacturing, but there is disagreement on the acceptable manufacturing offsets for CSPs. No defects were observed when thirty #1 test vehicles, each with 4 grid CSPs with 46 I/Os, were assembled.

Quality of Solder Joints

Figure 5 shows a SEM photomicrograph of a solder joint for a TAB CSP and a low I/O wafer level (8 I/O) package on a board for #1 TV. Low package height made inspection of the solder joints very difficult, either by visual or by SEM. Three

of these wafer packages showed poor quality solder joints with signs of cracking. Poor quality of the package was the reason for existence of microcracks after assembly. For these reasons, this package was excluded for the #2 test vehicle assembly.

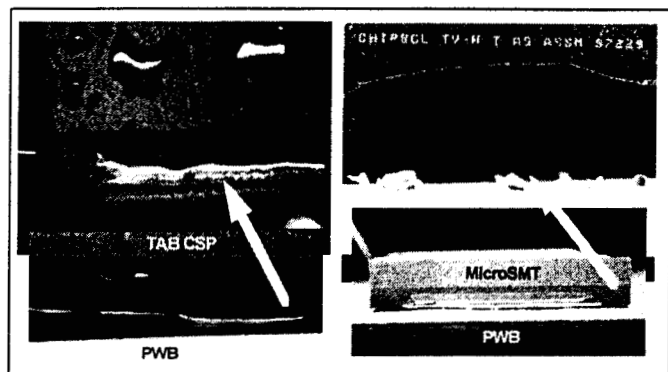


Figure 5 Good Solder Joint Quality of a Grid CSP and Poor Solder Joint Quality of Low I/O Wafer Level

Pull Test- As Assembled

Four of the TAB CSP-1 assemblies (#1 TV) were subjected to pull test after assembly prior to other environmental tests. The tensile loads were recorded for comparison and detached board/package surfaces were inspected for the failure mechanism. The following was found:

- No solder joint failures were observed; failures were at ball/package traces.
- The tensile forces for four assemblies were: 28, 25, 22, and 13 lb. The 13 to 28 lb. for a package of 46 I/Os is equivalent to 128 to 247 g/ball tensile strength. Shear forces for the same package before exposure to reflow process ranged from 320 to 400 g/ball (see Table 7 and Figure 2).

Pull Test – After Thermal Cycling

A number of #1 assembled test vehicles were subjected to thermal cycle A condition (-30°C/130°C). The CSP packages had internal daisy chains which made a closed loop with daisy chains on the PWB, enabling the monitoring of solder joint failures through interval electrical resistance measurement. Measurements were performed at room temperature on assemblies removed from the thermal cycling chamber. Cycles to failure were recorded.

After 1,500 cycles, several TAB CSP-1 assemblies were subjected to pull testing to determine strength degradation due to thermal cycling. In addition, failure sites and damaged areas were identified by using die penetrant prior to tensile test. The tensile loads for four test vehicles, each with four packages, are listed in Table 7 and plotted in Figure 6.

Tensile loads for thermally cycled assembled TVs ranged from 14 to 25 lb. force which are similar to the as assembled tensile test results. No significant decrease in tensile strength indicates that solder joints had minimal degradation due to 1,500 thermal cycles.

Balls failed at ball/package interface within traces as shown in Figure 7. There was no presence of dye penetrant on the fractured surfaces, i.e. no signs of solder joint damage or failures. This is a clear indication that failure due to thermal cycling, evident by the daisy chain opens for three assemblies, occurred within the package rather than in solder joints as commonly observed after thermal cycling.

No attempts were made to narrow the internal failure site since other investigators have identified the failure types for this package [3]. Failures have been reported to be from the TAB lead bond. Package internal failure might be true only for those fabricated from an early production version which were used in this test vehicle. This was verified by comparing the serial number on the package with the package supplier data base. The #2 TV includes packages from a more recent production version. This will help to determine if indeed improvement in cycles to failure reported by package supplier can be verified.

Table 7 Tensile forces before and after thermal cycling (1500 cycles, -30/100°C)

TAB CSP-1 46 I/O	Tensile Force As Assembled (lb force)	Tensile Force After 1,500 For 4 TVs (lb force)
A site	13	17,25,24*,23
B site	22	22,18,14,25*
C site	25	?,23*,18,20
D site	23	22,18,15,20

* Daisy chains were open at 1,500 cycles

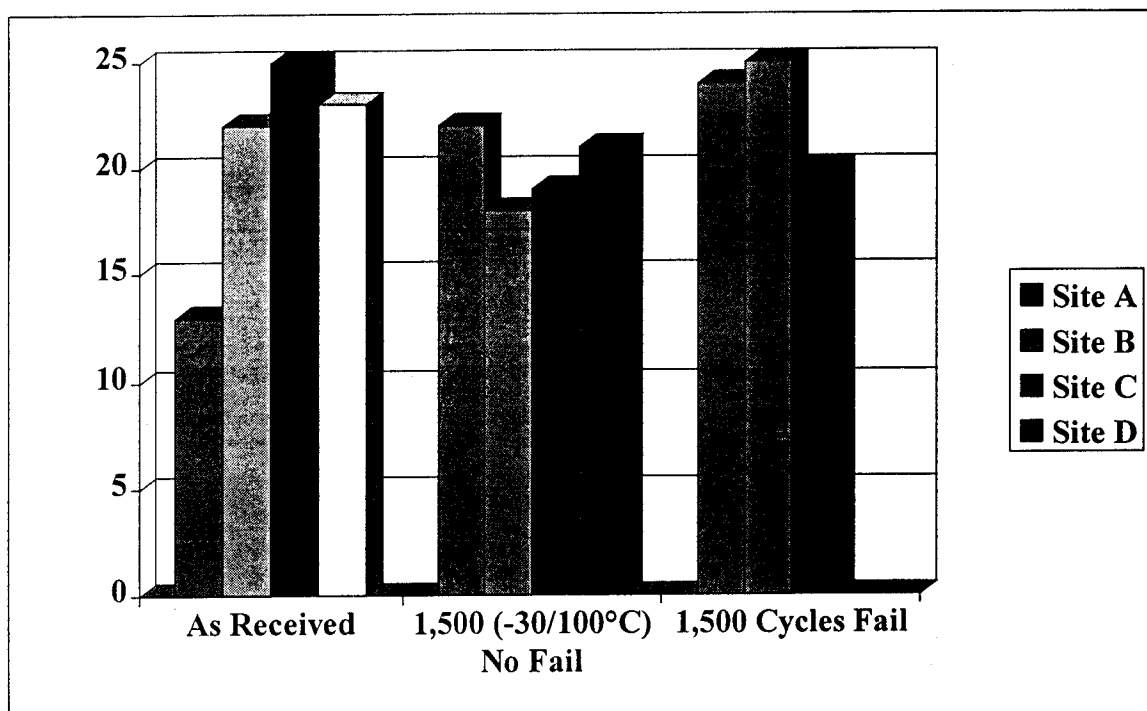


Figure 6 Pull Strength of Assembled TAB CSP with 46 I/O before and after 1,500 cycles

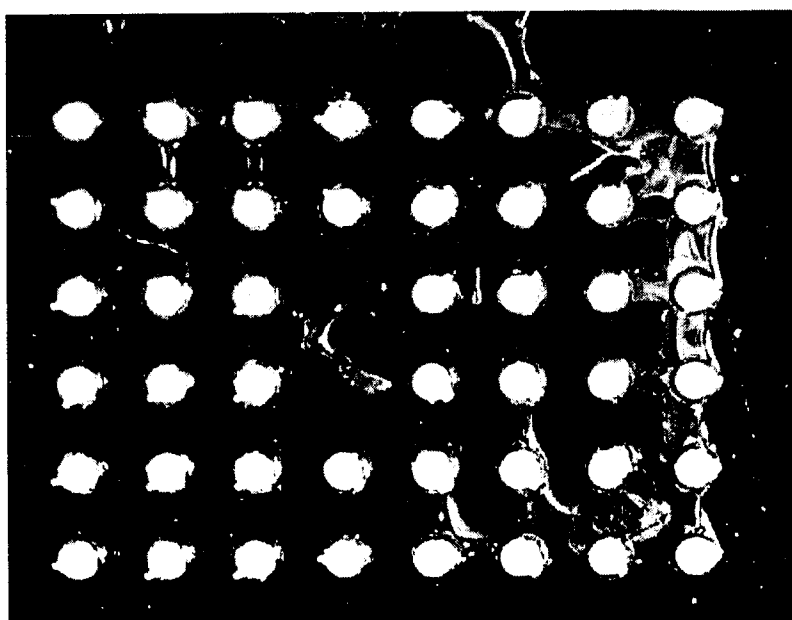


Figure 7 Die Penetrant of TAB CSP Assembly Failure with No Signs of Solder Joint Failure

Trial Thermal Cycling Test Results

Seven trial #2 test vehicles were assembled to optimize the assembly process and profile. The lowest stencil thickness, 4 mil, was used to determine the worst condition, that is, solder starving condition on a leadless package. A stencil thickness of 6 mil is the recommended thickness for assembly of leadless packages. One test vehicle was assembled double sided. Five of the PWBs had OSP surface finish, and two had HASL. All PWBs including the PWBs with HASL finish, were successfully assembled. As expected, working with HASL was much more difficult than OSP.

The five trial test vehicles with the OSP finish were subjected to thermal cycling in the range of -30 to 100°C (A condition). Both PWB and assembly conditions were not optimum for the trial test. Therefore, thermal cycling results may well suggest potential areas where the process can be optimized for the production test vehicle assemblies. Results are not valid for reliability and failure statistic analyses because of the low number of test samples and non-optimum condition.

For the trial test vehicle, automatic monitoring was impossible since connections to the ground plane were missed during file translation for PWB fabrication. This was corrected. For the full production assemblies, these daisy chains will be monitored continuously. For trial test vehicles, resistances were measured manually before and at different thermal cycling intervals to check for electrical opens (solder joint failure).

Table 8 shows resistances before and at different thermal cycles to 1,700 cycles. A number of assemblies were removed at different cycles for cross-section examination. Assemblies were periodically removed from the chamber and checked at room temperature (RT) for resistance (Ω). Continuous monitoring systems are being used for monitoring the full production assembly failures. The word "Open" in the Table indicates electrical open at RT and the word "STOP" indicates cycling discontinuation on the TV. Resistances are different for different daisy chain patterns, but are approximately the same for the same package on various test vehicle assemblies. It is interesting to note that even for non-optimum conditions, four out of six package assemblies survived to 700 cycles. Only two failed. Recall that the total number of packages for the full production is eleven.

Table 8 Daisy Chain Resistances of Assembled CSPs at Various Number of Cycles at Condition A (-30/100°C)

Package ID	Pkg ID	Pkg ID	Cycles 0	Cycles 100	Cycles 300	Cycles 400	Cycles 500	Cycles 600	Cycles 700	Cycles 900	Cycles 1000	Cycles 1200	Cycles 1500	Cycles 1700
Leadless-1	B	22-μvia	2.8	2.8	Open	Open	Open	Open	Open	Open	Open	Open	Open	STOP
Leadless-2	E	22-μvia	4.6	4.7	5.4	4.8	4.8	4.8	4.9	4.9	4.7	4.4	4.4	STOP
TAB CSP-1	F	22-μvia	9.3	9.2	9.5	9.3	9.4	9.5	9.6	9.4	9.5	9.1	9.2	STOP
TSOP 46 I/O	D	22-μvia	6.8	6.6	7	6.8	6.8	6.6	6.8	6.9	6.6	6.7	6.5	STOP
TAB CSP-2	C	22-μvia	5.8	5.7	6	6.2	5.7	5.9	5.8	5.9	5.7	5.7	5.6	STOP
Wafer Level	O-1	22-μvia	20.9	20.7	21.2	21.1	21.2	21.1	21.2	21.1	20.6	20.6	20.9	STOP
Wafer Level	O-2	22-μvia	23.7	23.5	23.8	23.7	23.6	23.7	23.8	23.9	23.4	23.3	23.4	STOP
Leadless-1	B	22-STD	2.3	2.3	2.6	2.7	2.6	2.4	Open	Open	Open	Open	Open	STOP
Leadless-2	E	22-STD	4	4.1	4.1	4.3	4.2	4.1	4.2	4.2	4	4.1	Open	STOP
TAB CSP-1	F	22-STD	9.3	9.3	9.4	9.4	9.2	9.2	9.6	9.6	9.5	9.1	9.2	STOP
TSOP 46 I/O	D	22-STD	5.9	6.3	5.9	6.2	5.8	5.8	6.2	6	6.1	5.8	5.7	STOP
TAB CSP-2	C	22-STD	6.1	6.2	6.9	6.6	6.9	6.3	6.6	7.1	45.8	1.4k	Open	STOP
Wafer Level	O-1	22-STD	Open	Open	Open	Open	Open	Open	Open	Open	Open	Open	Open	STOP
Wafer Level	O-2	22-STD	28.6	Open	Open	Open	Open	Open	Open	Open	Open	Open	Open	STOP
Leadless-1	B	29-STD	2.8	2.8	2.9	3	2.9	2.8	2.7	Open	Open	STOP	STOP	STOP
Leadless-2	E	29-STD	4.6	4.8	5.1	4.9	4.9	4.8	4.8	4.8	5	STOP	STOP	STOP
TAB CSP-1	F	29-STD	9.7	9.6	9.6	9.7	9.7	9.6	9.7	9.7	9.6	STOP	STOP	STOP
TSOP 46 I/O	D	29-STD	6.7	6.8	7	7	6.8	7	7	7	7	STOP	STOP	STOP
TAB CSP-2	C	29-STD	5.6	5.7	5.7	5.6	5.7	5.7	5.7	5.7	5.8	STOP	STOP	STOP
Wafer Level	O-1	29-STD	21.6	21.6	21.7	21.8	21	21.6	21.6	21.9	21.7	STOP	STOP	STOP
Wafer Level	O-2	29-STD	24.5	24.6	24.6	24.7	23.5	24.8	24.7	24.7	24.4	STOP	STOP	STOP
Leadless-1	B	3-STD	2.8	2.8	2.9	2.9	2.9	2.8	2.7	3	2.7	2.7	3	Open
Leadless-2	E	3-STD	4.7	4.7	4.9	5.1	4.8	4.7	4.8	4.9	4.7	4.5	4.7	4.1
TAB CSP-1	F	3-STD	9.5	9.4	9.6	9.7	9.6	9.8	9.5	9.8	9.7	9.9	9.6	9.2
TSOP 46 I/O	D	3-STD	6.8	6.7	7	7	7.1	6.9	6.9	7.5	7.1	6.7	6.6	6.7
TAB CSP-2	C	3-STD	5.7	5.6	6	5.9	5.9	5.6	5.9	210	58.6	1.4k	Open	Open
Wafer Level	O-1	3-STD	19.2	19.1	19.4	19.2	19.8	19.1	19.5	19.6	19.3	19	19	Open
Wafer Level	O-2	3-STD	22.8	22.6	22.9	22.9	22.7	22.6	23	23.1	23.3	22.6	Open	Open
Leadless-1	B	19-STD	2.8	2.7	2.9	3.2	2.9	STOP	STOP	STOP	STOP	STOP	STOP	STOP
Leadless-2	E	19-STD	4.8	4.7	5	4.6	4.7	STOP	STOP	STOP	STOP	STOP	STOP	STOP
TAB CSP-1	F	19-STD	10	10	10.1	10.3	10.6	STOP	STOP	STOP	STOP	STOP	STOP	STOP
TSOP 46 I/O	D	19-STD	6.8	6.8	6.9	6.7	6.5	STOP	STOP	STOP	STOP	STOP	STOP	STOP
TAB CSP-2	C	19-STD	7.8	Open	Open	Open	Open	STOP	STOP	STOP	STOP	STOP	STOP	STOP
Wafer Level	O-1	19-STD	23.3	23.3	23.3	23.7	24.7	STOP	STOP	STOP	STOP	STOP	STOP	STOP
Wafer Level	O-2	19-STD	24.8	24.7	24.8	25	23.3	STOP	STOP	STOP	STOP	STOP	STOP	STOP

The first failure was for the wafer level package (22-STD) with failure between 0 and 100 cycles. No underfill was used. This package is known to require underfill and those which were underfilled survived to 1500 thermal cycles.

The second failure was for the leadless package (22-μvia) which failed between 100 and 300 cycles from the μvia side. This package was mounted on a double sided assembly (22-STD and 22-μvia) with the microvia side (22-μvia) reflowed first, i.e., these joints were exposed to two reflows. In an effort to determine the cause of this early failure, it was also noticed that this is one of the packages that exactly overlapped another leadless package in the second side with a 90° rotation (see Fig. 8). The lay out for the double sided assembly was not mirror imaged. One image was rotated 90° relative to the first image.

During visual examination, it was noticed that the first failure location was at two cross-over corners. The criticality of solder disturbance at the crossing corners was verified in testing of the full production test vehicles and their Weibull plots are presented in the following. Early joint failure for double sided assemblies is qualitatively in agreement with another investigators' test results [4]. It was reported that a reduction of almost 50% in cycles to failure for double sided assemblies was seen with the mirror imaged packages. The number of cycles-to-failure was increased as double sided package assemblies moved away from the mirror position.

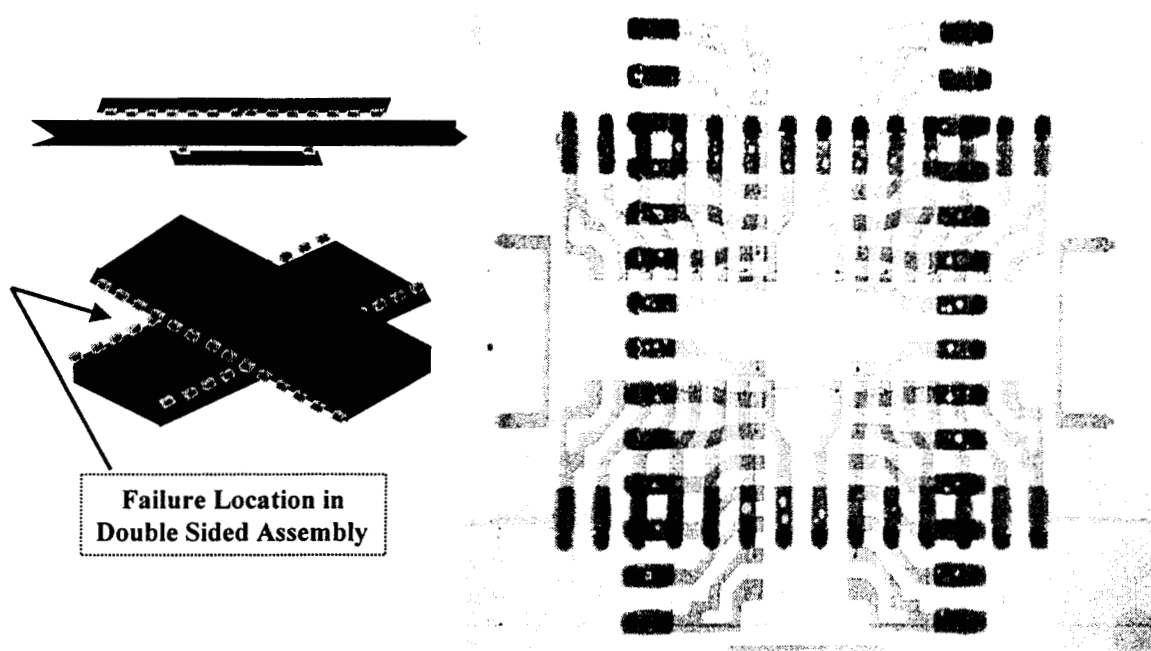


Figure 8 Solder Joint Failure Location in Double Sided Mirror-imaged Assemblies

The other failures of 22-STD (O-1), and 19-STD, were considered to be defect related, including package and PWB. The O-1 package was from the preproduction and provided for assembly purpose only. Via misregistration and solder mask coverage on the pads are other potential source of early failure. Recall that these test vehicles were from the trial run, the chief purpose of which was to understand the critical issues of PWB fabrication, process optimization, and daisy chain verification. Preliminary test results for a large number of assembled TVs from the 150 full production assemblies are presented in the following.

FULL PRODUCTION ASSEMBLY & RELIABILITY

The Consortium assembled different test vehicle types. For full production, about 150 test vehicles with the many variables discussed above were built. The photograph of an assembled test vehicle, with its packages, face up, is shown in Figure 9. A drawing for the Figure 9 double sided test vehicle in which the back side package outlines are also apparent is shown in Figure 10. Note that a few packages were mirror-imaged to another package in a double sided test vehicle.

Wide Distribution of Daisy Chain Resistances

The daisy chain resistance of an assembled package depends on both package and board design parameters. Once these parameters are set, resistances should fall within a narrow range. A relatively large (>20%) deviation from the norm value represents manufacturing defects.

Resistances for CSP assemblies were measured by a hand held multimeter and verified by two other team members at their facilities. Several unrealistically large resistance values were observed for three packages. Initially, it was thought that defects due to the daisy chain design might be the source. Further investigation revealed that the package production versions and package types were the cause of such variations.

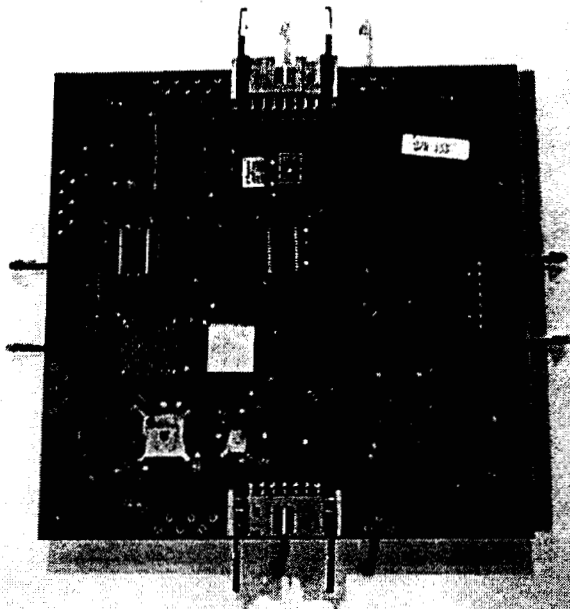


Figure 9 JPL Consortium Test Vehicle, Double Sided

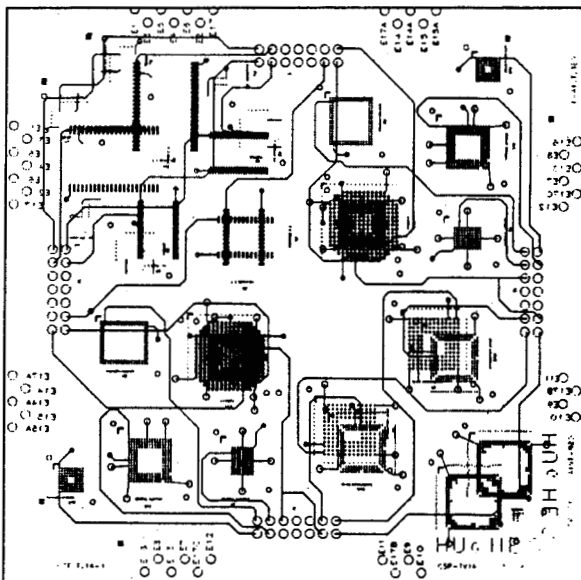


Figure 10 Double Sided Test Vehicle and Regions of Package Overlaps

Figure 5 presents the cumulative distribution of resistance values for nine package assemblies. A small deviation from the norm values are acceptable since these were measured manually. A noticeable high resistance values represent most probably a manufacturing defect. These are shown by arrows towards the top end cumulative distributions in Figure. Assemblies with such defects are expected to fail much earlier than their norm. In our case, several of manufacturing variables were intentionally introduced to determine the effects of such variables on reliability. Two of manufacturing variables were change of stencil thickness and placement offsets.

Effects of package lot source apparent from J144, wire-on-flex (WOF), plots of accumulative daisy chain resistance. One set had a resistance value of about $2\ \Omega$ and the other about $87\ \Omega$, each with relatively a narrow distribution. The package lot was apparent from a marking on the package for each category; therefore, the possibility that such variations were due to board or assembly was rejected. Package K176, WOF, from the same vendor showed a more narrower resistance distribution. Resistance values were higher than J144, but their values were close to one of the lot source.

Resistance values for M206, chip-on-flex (COF), were unrealistically high, nearly $700\ \Omega$. Resistance measurement of two adjacent balls within the package were high, narrowing the cause of high value to package. These results may indicate that

the trace fabrication process for this technology is the source of high resistance. Further comparison of results for the JPL CSP consortium will further shed light on these issues.

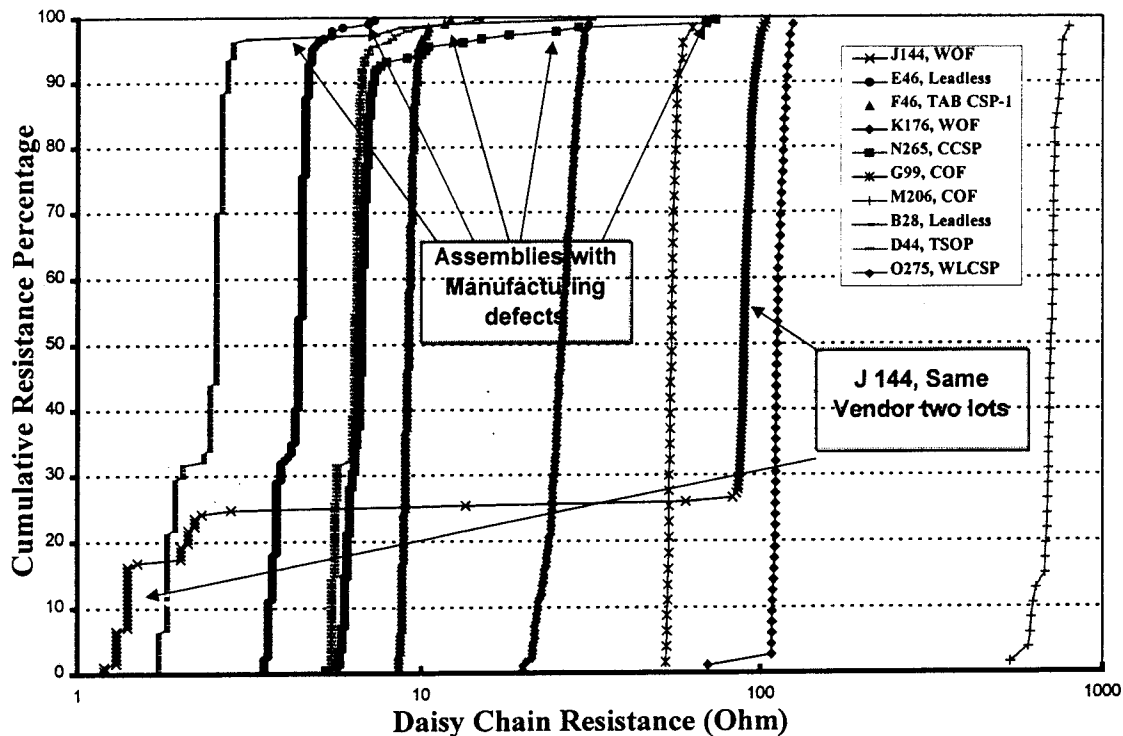


Figure 10 Cumulative Resistance for CSP Assemblies,

Environmental Test Results

A large number of assemblies have already failed, and their cycles to failure have been documented. Out of these, cycles to failure data for three packages under four thermal cycling conditions are reviewed. Results for two chip on flex assemblies and leadless assemblies on single and double sided test vehicles are also presented.

Cycles to Failures for Chip on Flex Assemblies

Figure 11 shows cycles to failure for the two chip-on-flex packages with two different I/Os under the same thermal cycling conditions. Test results are for 99 I/O and 206 I/O packages subjected to cycle A condition (-30/100°C). The cycles to failure distribution for the higher I/O assembly is much narrower than its lower I/O package. One may even note two possibly distinct failure distribution for the G99 I/O assemblies. The reason for the two failure trends are yet to be identified.

Figure 12 compares cycles to failure test results for the G package with 99 I/Os under four thermal cycling conditions. The trends are as expected, i.e., as the thermal cycling temperature ranges increase, the cycles to failure decrease. Note that assemblies failed between 3 to 34 cycles under a near thermal shock in the range of -55 to 125 °C (B condition). Cycles to failure was 152 cycles under a typical commercial thermal cycling conditions in the ranges of 0 to 100°C. Results for -55/100°C and -30/100°C were between the two extreme cycling conditions as expected.

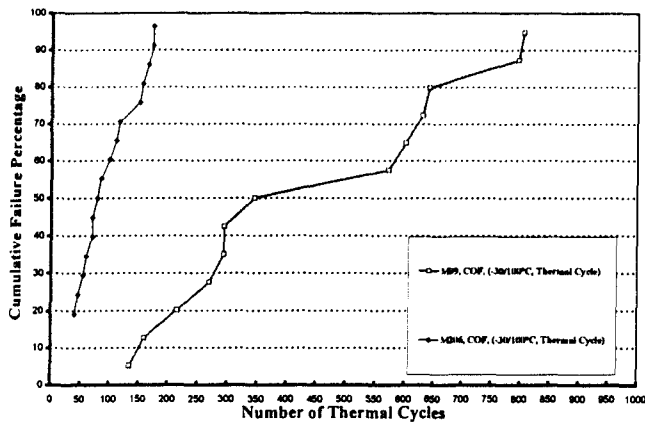


Figure 11 Cumulative Failure Distribution for Flex on Chip Assemblies with 99 and 206 I/Os

These data will be used to see the effects of both maximum and minimum temperature changes as well as how well they will follow projection models such as Coffin-Manson relationship.

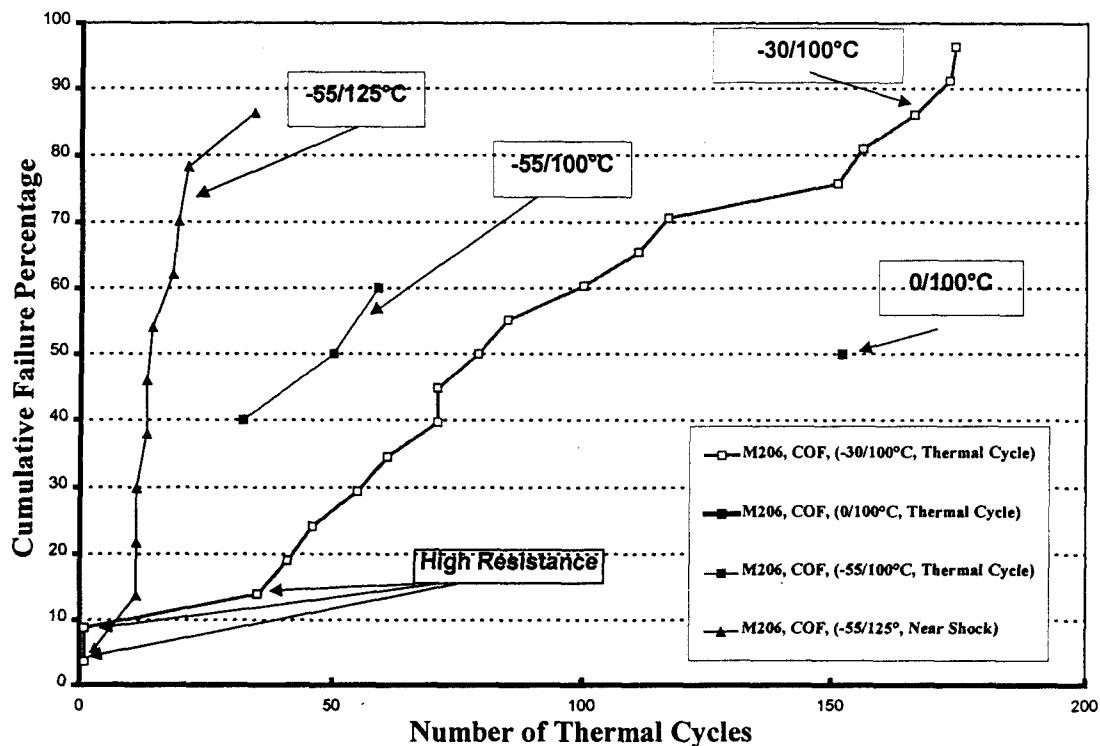


Figure 12 Cumulative Failure Distribution for Flex on Chip Assemblies with 206 I/Os Under Four Thermal Cycle Conditions

X-ray Inspection under Exaggerated Condition

One M206 assembly which failed at 35 cycles in the range of -30/100 was inspected after it was further cycled to 500. By further cycling, we were able to exaggerate the cracking and separation of solder balls/joint. This allowed the clear observation of solder joint openings that are generally impossible to detect when they have just failed. Figure 13 shows an

X-ray photomicrograph of an exaggerated failure. It is apparent that separation occurred either from the package site or board site

Single and Double Sided Mirror-imaged

Figure 14 shows thermal cycling test results for package B, a leadless assembly with 28 I/Os, under two conditions for both single and double sided assemblies. The assembly location on the board was such that in a double sided assembly, it was a direct mirror image of itself with a 90° rotation (see Figure 9).

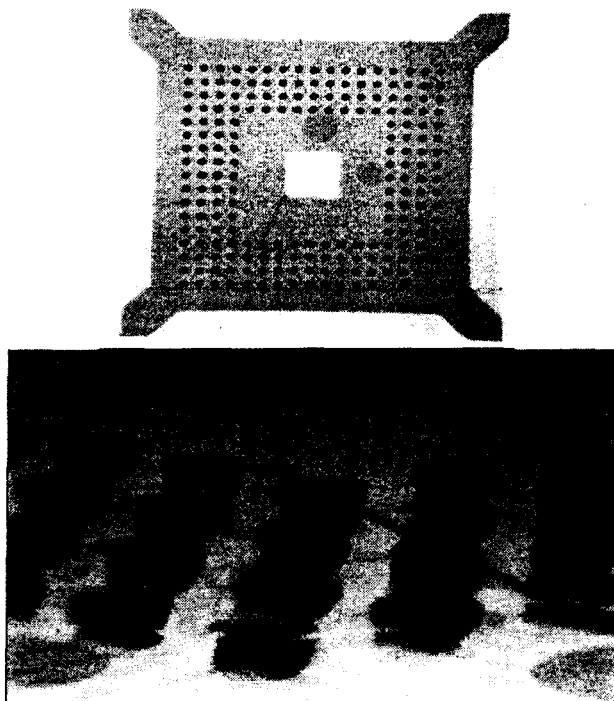


Figure 13 Exaggerated X-rays showing failure from either package or board sites

The single sided assemblies failed at much higher cycles than double sided assemblies. The N50 (cycles to 50% failure) were 437 for double and 763 for single sided assemblies under cycle A condition (-30/100 °C). The double sided assemblies also failed much earlier than single sided assemblies under other thermal cycling conditions. As an example, results for double sided assemblies under -55/125°C is also included in the Figure.

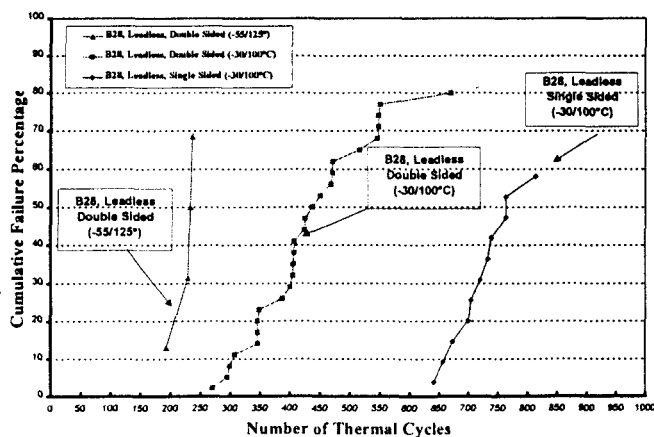


Figure 14 Single and Double Sided Assembly Failure Comparison

CONCLUSIONS

- Ball/package failure shear forces were much lower for CSPs than BGAs. In general, forces increased after isothermal aging at 100°C to 1,000 hours, and then leveled off or slightly decreased to 2,000 hours. For aging at 125°C to 1,000 hours, for a few cases, forces dropped by 40% and then leveled off or decreased to 2,000 hours.
- Traditionally, solder joint failure was considered to be the weakest link in the microelectronics attachment reliability. This might not be true for CSPs with innovative designs and the use of new materials and processes. For example, the internal package TAB lead bond failure was considered to be the possible cause of a CSP failure after cycling.
- The solder joints which were reflowed twice, in a double sided assembly, showed earlier failures. For a leadless package, this was further worsened by package back to back (mirror image) assembly.
- Cycles to failure for the same assembly under four different environments were different, but the trends were as expected. This means, as temperature cycling ranges increased, cycles to failure decreased.
- One package required underfilling, and three others showed very low cycles to failures. Underfilling might be a requirement for these packages even for relatively benign commercial application.

For wider CSP implementation, meaningful reliability data are needed. Accelerated thermal cycling might be severe and introduce failure mechanisms that are not representative of field applications. Complimentary tests and failure analyses need to be performed to build confidence in assembly reliability. Thus, understanding the overall philosophy of qualification testing to meet system requirements as well as detecting new failure mechanisms associated with the miniaturized CSPs is the key to collecting meaningful test results and building confidence in its implementation.

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Table 1 CSPs Assembly Reliability, Flex/Rigid Interposer

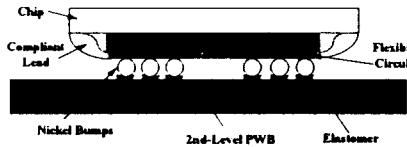
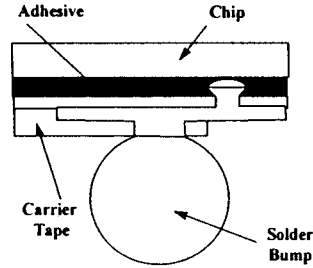
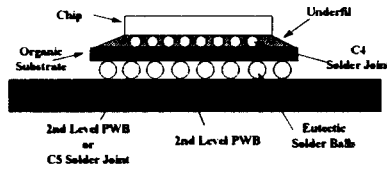
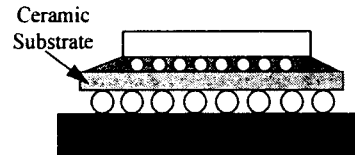
Package Schematic (not to scale)	Package Type	Cycling Condition	Total Cycles	Fails/ Samples	I/O	References
	μBGA (Tessera) Intel Test Data	-65°C to 150°C -55°C to 125°C	750 1000 1000 no underfill	0/78 4/78* 0/78	46	S. Greathouse, "Chip Scale Package Solutions-The Pro's and Cons," Proceedings of second International Conference on Chip Scale Packaging, CHIPCON '97, Feb. 20-21, 1997 * 4/78 right after 1,000 cycles in lead
	μBGA Motorola Test	-55°C to 125°C 5.8 cycles/hr	500* 600	1/8 3/8	40	Lall, P., "Assembly Level Reliability Characterization of Chip-Scale Packages," 48th Electronic Component & Technology Conference, May 25-28, 1998 * Internal TAB failure
	FPBGA (NEC)	-40°C to 125°C	200 underfill	0/20	232	S. Matsuda, K. Kata, E. Hagimoto, "Simple-Structure, Generally Applicable Chip-Scale Package," Proceeding of IEEE Electronic Components & Technology Conference, May 1995, P. 218-223
		-55°C to 125°C 10 min. dwells -40°C to 125°C*	700 underfill 500 No underfill	N/A 0/12	208 44	T. Oishi, et al, "Strategy for Fine Pitch BGA Development in NEC, and its Applications," Proceedings of second International Conference on Chip Scale Packaging, CHIPCON '97, Feb. 20-21, 1997 *Presentation, CHIPCON '97
 	JACS-Pak (Motorola)	-40°C to 125°C (1 Cycle/hr, 10 min. dwells) -55°C to 125°C Shock, 5 min. dwells	>1150* no underfill 1300**	NA 1st Failure	80 80	C. Koehler, et al, "A User-Focused Chip Scale Packaging Solution," Proceedings of second International Conference on Chip Scale Packaging, CHIPCON '97, Feb. 20-21, 1997 * >600 in paper, but >1150 presentation ** >1100 in paper, but 1300 1st failure presentation
	Ceramic CSP (Kyocera)	-40°C to 125°C	~600 no underfill, PWB 0.6mm >900 no underfill, PWB 1.6mm	NA	220	R. Lanzone, "Ceramic CSP: A Low Cost, Adaptive Interconnect, High Density Technology," Proceedings of second International Conference on Chip Scale Packaging, CHIPCON '97, Feb. 20-21, 1997 Private Communication

Table 2 CSPs Assembly Reliability, Wafer Level

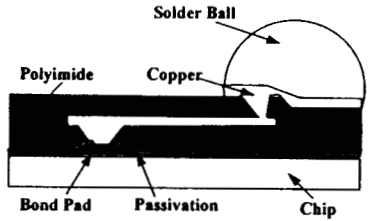
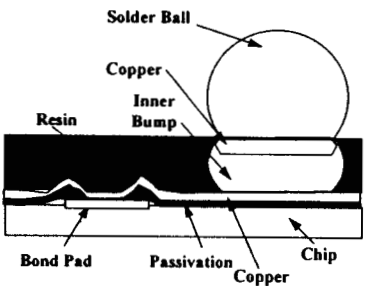
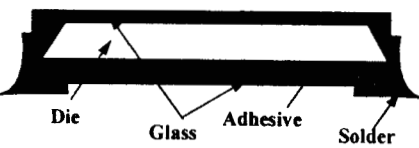
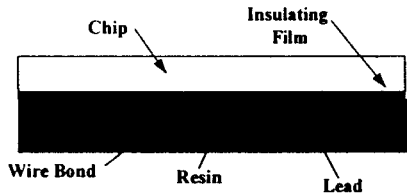
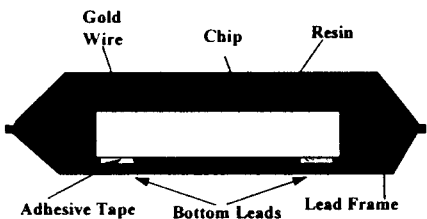
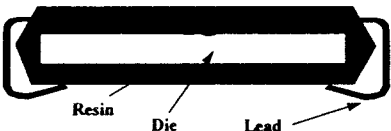

Package Schematic (not to scale)	Package Type	Cycling Condition	Total Cycles	Fails/ Samples	I/O	References.
 <p>Solder Ball Polyimide Copper Bond Pad Passivation Chip</p>	miniBGA (Sandia)	<p>0°C to 100°C (Thermal Shock)</p> <p>-55°C to 125°C Thermal Shock 15 min. dwells</p>	<p>>2000 underfill <40 no underfill >500 underfill</p>	NA	266	R. Chanchani, et al, "mini Ball Grid Array (mBGA) Assembly on MCM-L Boards," Proceedings of Electronic Components and Technology Conference, May 18-21, 1997
 <p>Solder Ball Copper Inner Bump Resin Bond Pad Passivation Copper Chip</p>	Mitsubishi	-40°C to 125°C, 1 cycle/hour	<p>500 underfill 200 no underfill 100 bare die</p>	<p>0/3 (0/20) 10/30</p>	96	S. Baba, et al, "Molded Chip Scale Package for High Pin Count," Proceeding of IEEE Electronic Components & Technology Conference, May 1996, P. 1251-1257
 <p>Die Glass Adhesive Solder</p>	Shell Case Peripheral	<p>-45°C to 85°C 10 min., 1 min. between (Thermal Shock)</p>	<p>1000 10x10 mm die 8x13</p>	<p>0/24 65 μ stand off 0/40 130 μ stand off</p>	120	Presentation- A. Badihi, "Test Results for Reliability of ShellCase CSPs," IMAPS ATW Workshop on CSP, August 10-12, 1997, Austin, Texas

Table 3 CSPs Assembly Reliability Lead On Chip

Package Schematic (not to scale)	Package Type	Cycling Condition	Total Cycles	Fails/ Samples	I/O	References
	LOC-USON (Fujitsu) LOC ultra-thin small outline no-lead	-65°C, 30 min. to 155°C, 30 min.	500	0/40	26	J. Kasai, et al, "Low Cost Chip Scale Package for Memory Products," Surface Mount International, August 29-31, 1995
	LOC (BLP) LGSemicon TSOP	-30°C 85°C -55°C to 125°C Shock, 5 min. dwells -55°C to 125°C Shock, 5 min. dwells	>1200 800 900 900 1000	N/A 0/4 2/4 0/25 2/25	20 28 28	Y. Kim, et al, "Bottom Ledged Plastic (BLP) Package: A New Design with Enhanced Solder Joint Reliability," Proceeding of IEEE Electronic Components & Technology Conference, May 1996, P. 448-452 Y. Kim, et al, "Solder Joint Reliability of The Leaded and Leadless Packages: New BLP Design," SEMICON West, July 18-21, 1997
	Hitachi Cable LOC	-50°C 150°C 30 min., 10 min. between	>1000	No crack	44	K. Hatano, et al, "Reliability of CSP Manufactured by Using LOC Package Technology," IMAPS ATW Workshop on CSP, August 10-12, 1997, Austin, Texas
	TSOP	-55°C to 125°C -55°C to 125°C 0°C to 100°C 0°C to 100°C	2,200 200 735 750	1st Failure 1st Failure 1st Failure 1st Failure	32 32 32 32	J. Lau, editor, "Solder Joint Reliability Theory and Applications R. Darveau P. Viswanadham, et al, "Solder Joint Reliability on TSOPs-An Overview", IEEE 43rd ECTC, P 883, 1993 D. Noctor, et al, IEEE Trans on CHMT, Vol. 16, No.6, 1993